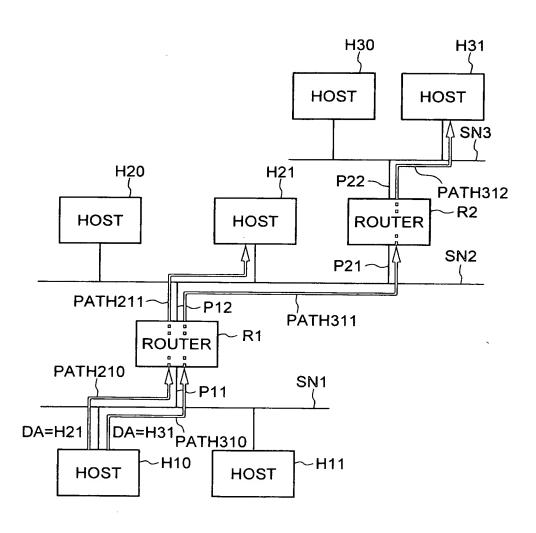
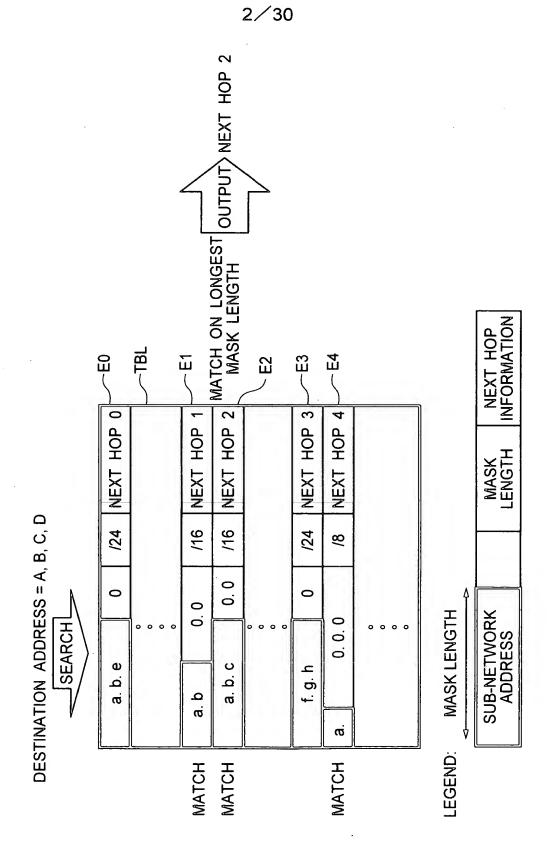
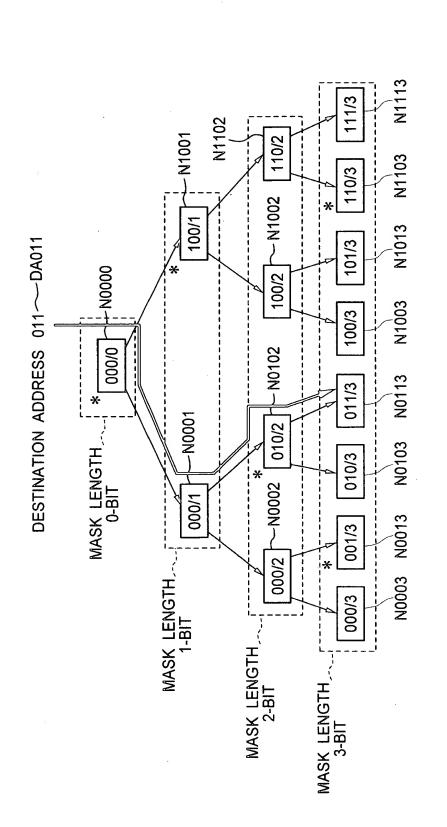
FIG. 1







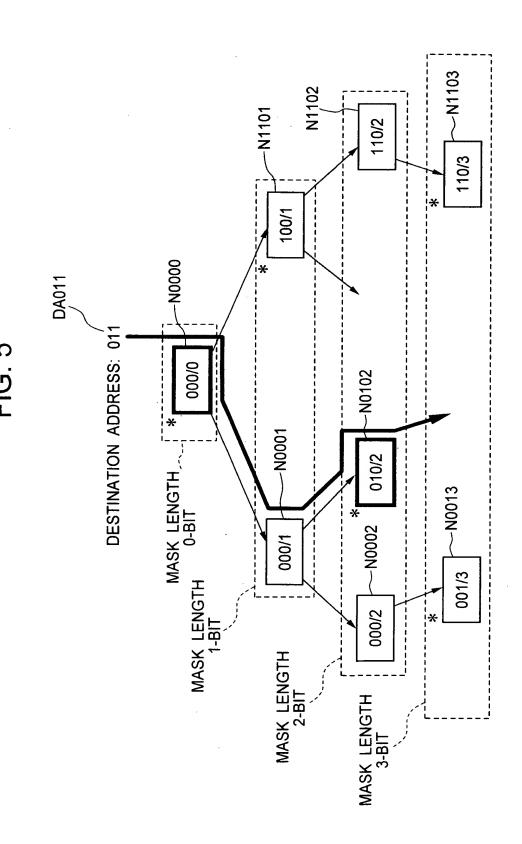
INDICATES THAT A PATH IS ALLOCATED TO THIS NODE.

SUB-NETWORK ADDRESS/MASK LENGTH

LEGEND:

SUB-NETWORK ADDRESS	/	MASK LENGTH
000	1	0
001	/	3
010	/	2
100	1	1
110	1	3
		1





A STATE OF THE STA

FIG. 6

PATH TABLE

/	MASK LENGTH
/	0
/	16
/	16
	/

7/30 FIG. 7

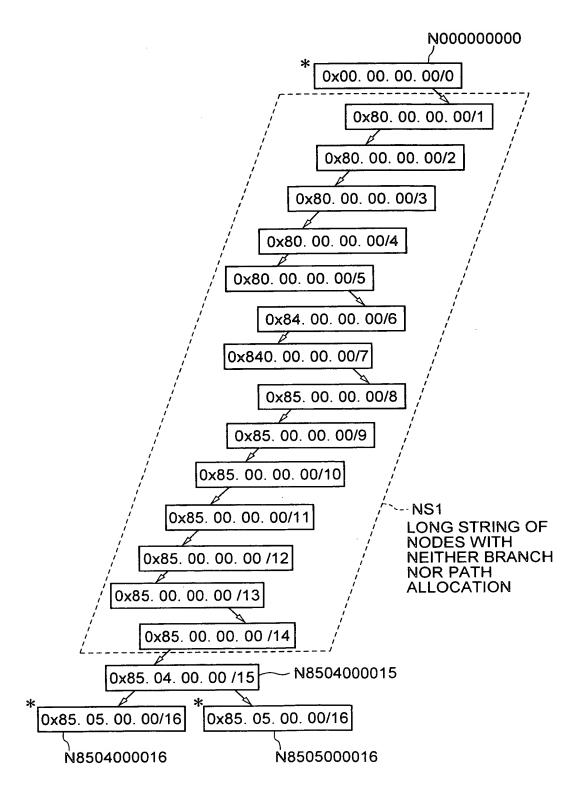


FIG. 8

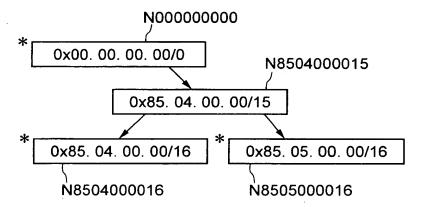
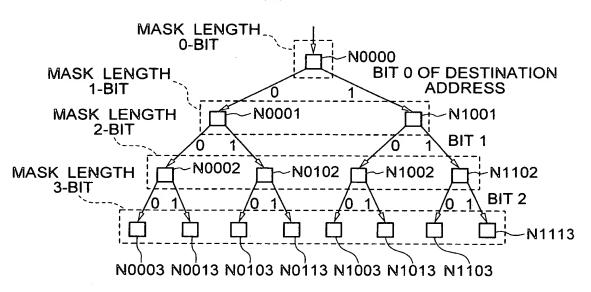
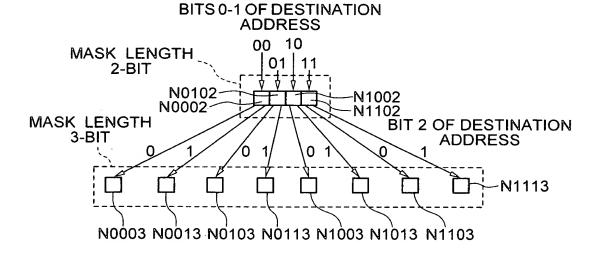


FIG. 9

(a)

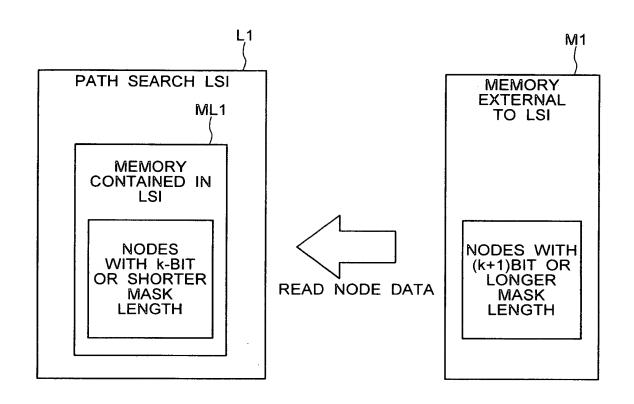


(b)



ļ. #

FIG. 10





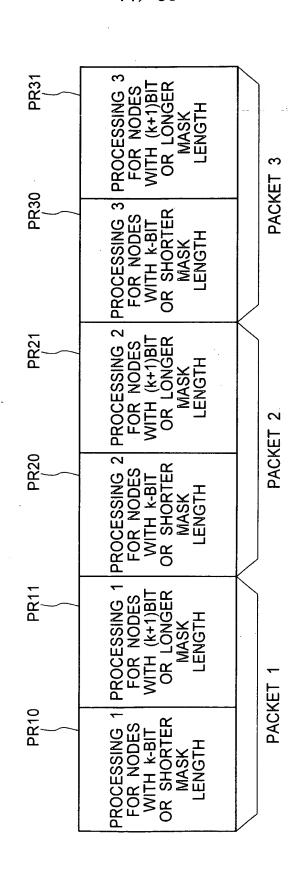


FIG. 12

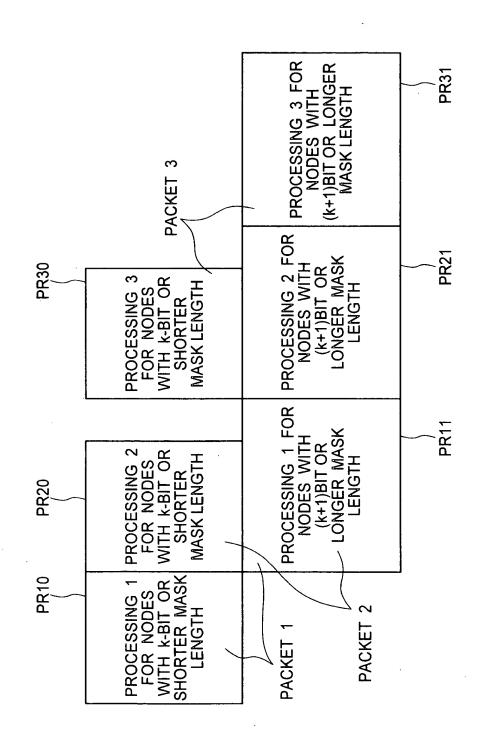


FIG. 13

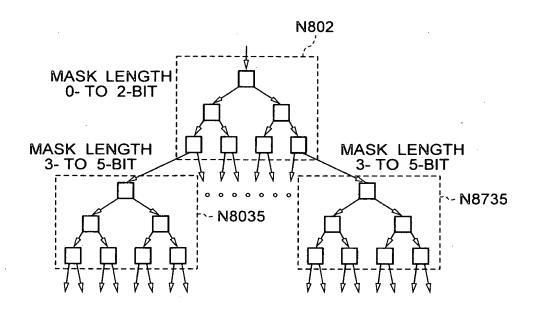


FIG. 14

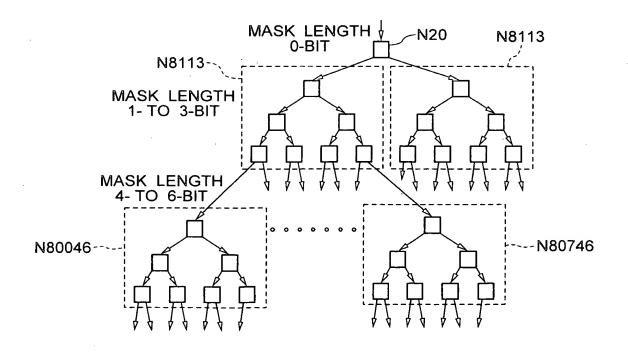


FIG. 15

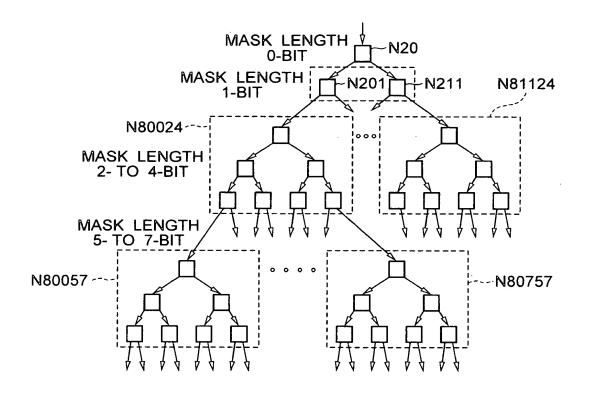


FIG. 16

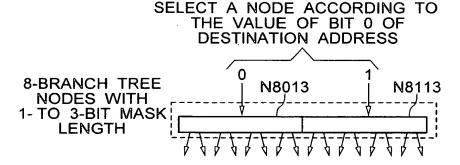


FIG. 17

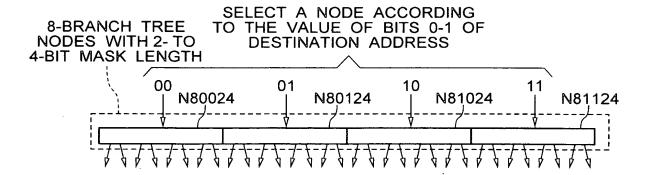


FIG. 18

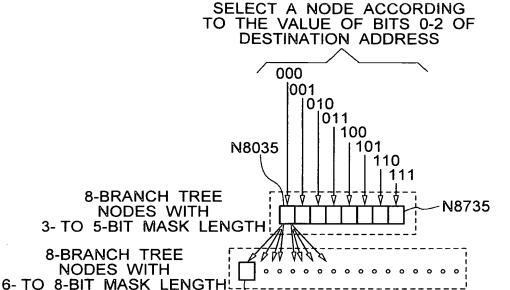


FIG. 19

N80068

SELECT A NODE ACCORDING TO THE VALUE OF BITS 0-3 OF DESTINATION ADDRESS

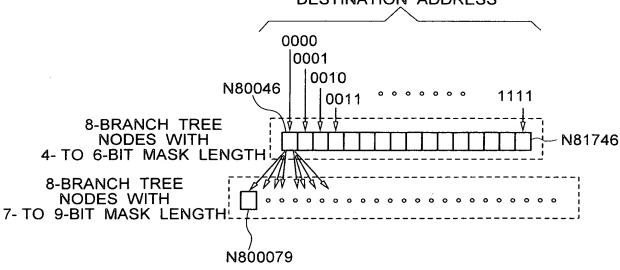


FIG. 20

SELECT A NODE ACCORDING TO THE VALUE OF BITS 0-4 OF DESTINATION ADDRESS

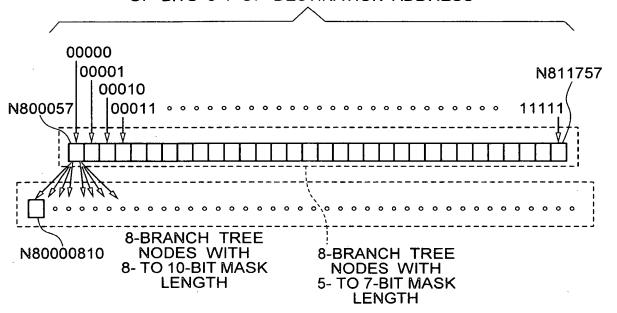
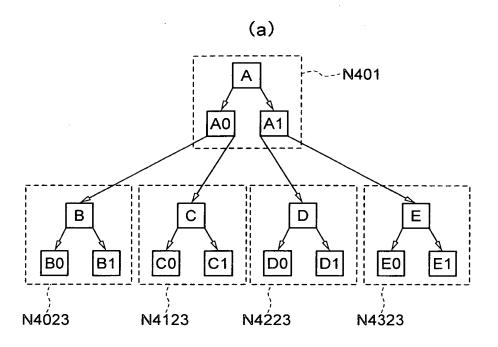
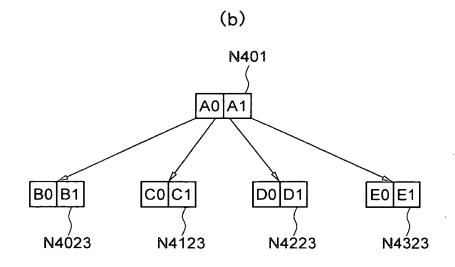


FIG. 21





19/30 **FIG**. **22**

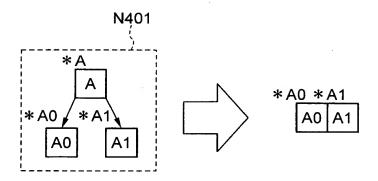


FIG. 23

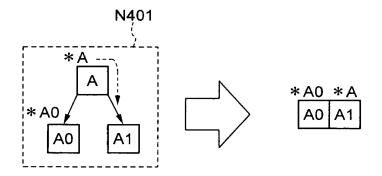
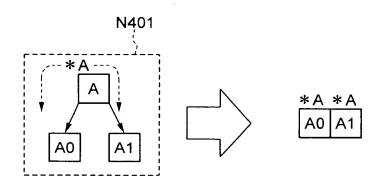


FIG. 24



20/30 FIG. 25

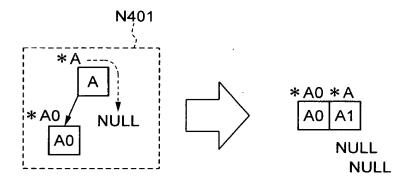


FIG. 26

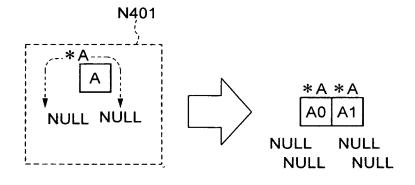


FIG. 27

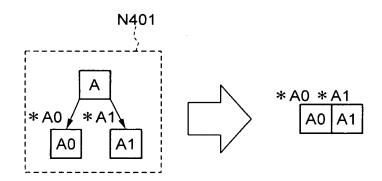


FIG. 28

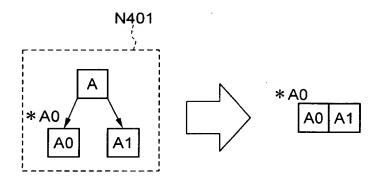


FIG. 29

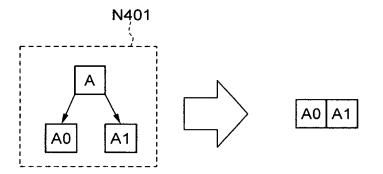
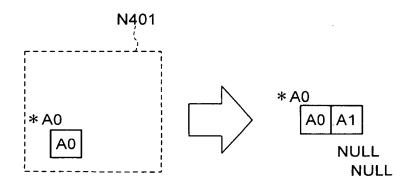


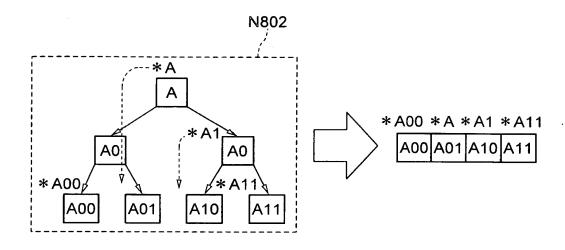
FIG. 30



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FIG. 31

(a)



(b)

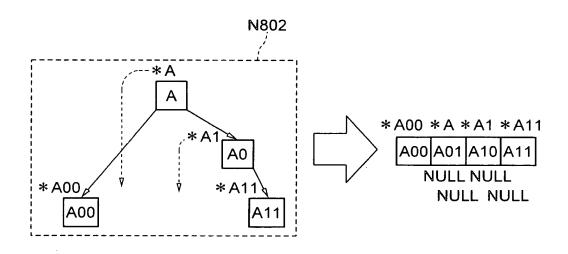


FIG. 32

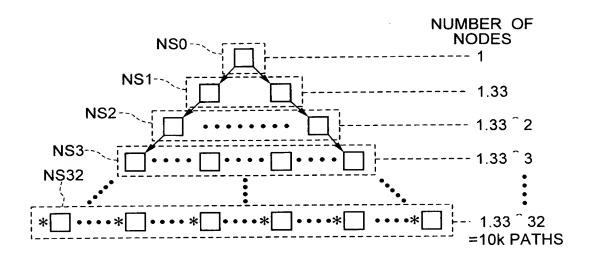
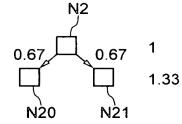


FIG. 33

(a)



AVERAGE: 1 + 1.33 = MEMORY AMOUNT FOR 2.33 2-BRANCH TREE NODES

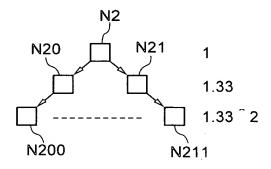
2-BRANCH TREE NODE

N4 N20 N21

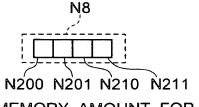
MEMORY AMOUNT FOR 2 2-BRANCH TREE NODES

4-BRANCH TREE NODE

(b)



AVERAGE: 1 + 1.33 + 1.33 ^ 2= MEMORY AMOUNT FOR 4.11 2-BRANCH TREE NODES 2-BRANCH TREE NODE



MEMORY AMOUNT FOR 4 2-BRANCH TREE NODES

8-BRANCH TREE NODE

FIG. 34

32 BITS

W0	NEXT NODE MASK LENGTH 0	FLAG 0	POINTER 0 TO NEXT NODE			
W1	NEXT NODE MASK LENGTH 1	FLAG 1	POINTER 1 TO NEXT NODE			
W2	SUB-NETWORK ADDRESS					
W3	NEXT-HOP ADDRESS					
W4	OUTPUT PORT	R				

2-BRANCH TREE NODE

of their sign

FIG. 35

32 BITS

W0	NEXT NODE MASK LENGTH 00	FLAG 00	PC	DINTER 00 TO NEXT NODE		
W1	NEXT NODE MASK LENGTH 01	FLAG 01	PC	DINTER 01 TO NEXT NODE		
W2	NEXT NODE MASK LENGTH 10	FLAG 10	POINTER 10 TO NEXT NODE			
W3	NEXT NODE MASK LENGTH 11	FLAG 11	POINTER 11 TO NEXT NOD			
W4	SUB-NETWORK ADDRESS					
W5	OUTPUT PORT NUMBER 0			OUTPUT PORT NUMBER 1		
W6	NEXT HOP ADDRESS 0					
W7	NEXT HOP ADDRESS 1					
•						

4-BRANCH TREE NODE

FIG. 36

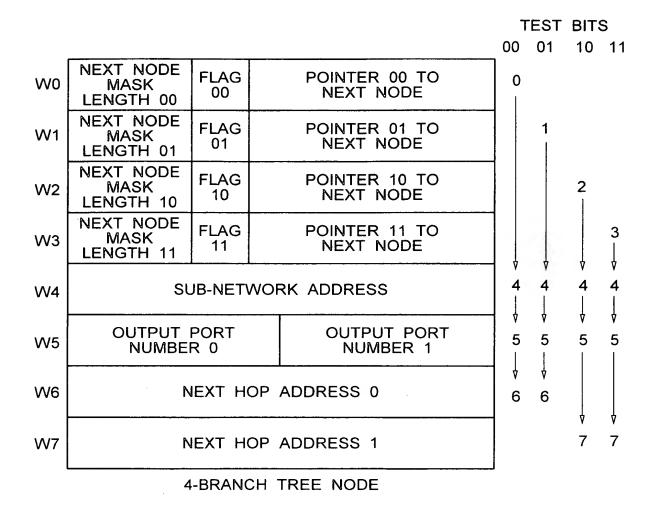


FIG. 37

							TEST BITS				
					00	01	10	11			
Wo	NEXT NODE MASK LENGTH 00	FLAG 00		POINTER 00 TO NEXT NODE	0						
W1	NEXT NODE MASK LENGTH 01	FLAG 01		POINTER 01 TO NEXT NODE		1					
W2	NEXT NODE MASK LENGTH 10	FLAG 10		POINTER 10 TO NEXT NODE			2				
W3	NEXT NODE MASK LENGTH 11	FLAG 11		POINTER 11 TO NEXT NODE				3			
W4	SUB-NETWORK ADDRESS						4	4			
W5	OUTPUT PORT NUMBER 0			OUTPUT PORT NUMBER 1							
W6	NEXT HOP ADDRESS 0										
W7	NEXT HOP ADDRESS 1										
4-BRANCH TREE NODE											

FIG. 38

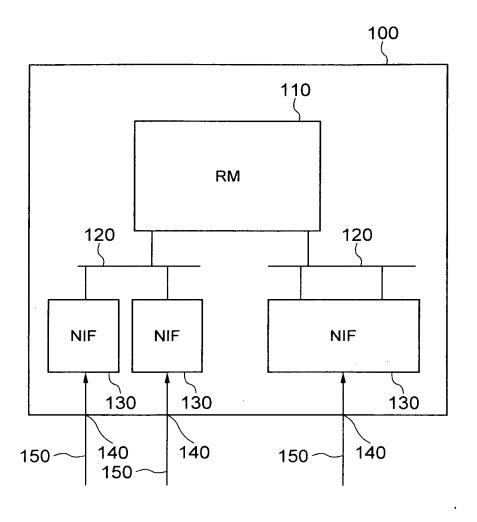


FIG. 39

